AzureWave Technologies, Inc.

AW-CU480

Bluetooth Low Energy 5.0 wireless microcontroller Stamp LGA module

Datasheet

Rev. E

DF

(For STD)

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Features

Benefits

- Very low current solution for long battery life
- Single chip device to run stack and application
- System BOM is low in component count and cost
- Flexible sensor interfacing
- Embedded NTAG

Radio

- 2.4 GHz Bluetooth Low Energy 5.0 compliant
- Bluetooth Low Energy 5.0 2Mbps high data rate
- Improved co-existence with WiFi
- 1.9 V to 3.6 V supply voltage
- Antenna Diversity control
- 32 MHz XTAL cell with internal capacitors, able with suitable external XTAL to meet the required accuracy for radio operation over the operating conditions
- Integrated Ultra Low-power sleep oscillator
- 128-bit, 192-bit or 256-bit AES security processor

Microcontroller

- Application CPU, Arm Cortex-M4 CPU:
    - Arm Cortex-M4 processor, running at a frequency of up to 48 MHz.
    - Arm built-in Nested Vectored Interrupt Controller (NVIC)
    - Memory Protection Unit (MPU)
    - Non-maskable Interrupt (NMI) with a selection of sources
    - Serial Wire Debug (SWD) with 8 breakpoints and 4 watch points
    - System tick timer
    - Includes Serial Wire Output for enhanced debug capabilities.
- On-Chip memory
    - 640 KB flash
    - 152 KB SRAM
- 12 MHz to 48 MHz system clock speed for low-power
- 2 x I2C-bus interface, operate as either master or slave
- 10 x PWM
- 2 x Low-power timers
- 2 x USART, one with flow control
- 2 x SPI-bus, master or slave
- 1 x PDM digital audio interface with a hardware based voice activity detector to reduce
- Power consumption in voice applications. Support for dual-channel microphone
- Interface, flexible decimators, 16 entry FIFOs and optional DC blocking.
- 18-channel DMA engine for efficient data transfer between peripherals and SRAM, or SRAM to SRAM. DMA can operate with fixed or incrementing addresses. Operations can be chained together to provide complex functionality with low CPU overhead.
- Up to four GPIOs can be selected as pin interrupts (PINT), triggered by rising, falling or both input edges.
- Two GPIO grouped interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
- 32-bit Real Time clock (RTC) with 1 s resolution.

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A timer in the RTC can be used to wake from Sleep, Deep-sleep and Power-down, with 1 ms resolution

- Voltage Brown Out with 8 programmable thresholds
- 8-input 12-bit ADC, 190 kS/sec. HW support for continuous operation or single conversions, single or multiple inputs can be sampled within a sequence. DMA operation can be linked to achieve low overhead operation.
- 1 x analog comparator
- Battery and temperature sensors
- Watchdog timer and POR
- Standby power controller
- Up to 22 Digital IOs (DIO)
- 1 x Quad SPIFI for accessing an external flash device either through register accesses or for direct execution of code
- Random Number Generator engine
- AES engine AES-128 to 256
- Hash hardware accelerator supporting SHA-1, SHA-256
- EFuse:
    - 128-bit random AES key
    - configuration modes
    - Trimming
- ISO7816 smart card digital interface which with a suitable external analogue device can operate as a smart card reader

Low power

- Sleep mode supported, the CPU in low power state waiting for interrupt
- Deep-sleep mode supported, the CPU in low power state waiting for interrupt, but extra functionality disabled or in low power state compared to sleep mode
- Power Down mode, main functionality powered down, wakeup possible from IOs, wakeup possible from some peripherals (I2C, USART, SPI) in a limited function mode and low power timers
- Deep -power down, very low power state with option of wake-up triggered by IOs, 350nA
- 41-bit and 28-bit Low power timers can run in power down mode, clocked by 32 kHz FRO or 32 kHz XTAL. Timers can run for over one year or 2 days
- Dedicated low power timer, clocked by 32 kHz XTAL, closely integrated with the Bluetooth Low Energy link layer to maintain the timing reference through power-down Cycles

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Revision History

Document NO: R2-2480-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
A	2020/4/24	DCN017199	● Initial Version	Shihhua Huang	NC Chen
B	2020/6/22	DCN017594	● Removed watermark	Shihhua Huang	NC Chen
C	2020/7/2	DCN017678	● Correct BT output power	Shihhua Huang	NC Chen
D	2020/12/4	DCN019430	● Modify chapter 1.3 info ● Update power consumption	Shihhua Huang	NC Chen
E	2021/4/13	DCN021243	*Changed to new format ● Modify Block Diagram	Shihhua Huang	NC Chen

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1. Introduction

1.1 Product Overview

AzureWave Technologies, Inc. introduces the advanced Bluetooth Stamp LGA module---AW-CU480. The AW-CU480 is ultra-low power, high performance Arm® Cortex®-M4 based wireless microcontrollers supporting Bluetooth Low Energy 5.0 to facilitate the development of Bluetooth Low Energy applications.

The AW-CU480, supporting eight simultaneous connections, includes a 2.4 GHz Bluetooth Low Energy 5 compliant transceiver and a comprehensive mix of analog and digital peripherals. Ultra-low current consumption in both radio receive and transmit modes and also in the power down modes allow use of coin cell batteries.

The product has 640 KB embedded Flash, 152 KB RAM memory. The embedded flash can support Over the Air (OTA) code download of applications. The devices include 10-channel PWM, two timers, one RTC/alarm timer, a Windowed Watchdog Timer (WWDT), two USARTs, two SPI interfaces, two I2C interfaces, a DMIC subsystem with dual-channel PDM microphone interface with voice activity detector, one 12-bit ADC, temperature sensor and comparator.

The AW-CU480 variant has an internal NFC tag and with connections to the external NFC antenna.

The Arm Cortex-M4 is a 32-bit core that offers system enhancements such as low power consumption, enhanced debug features, and a high level support of the block integration. The Arm Cortex-M4 CPU, operates at up to 48 MHz.

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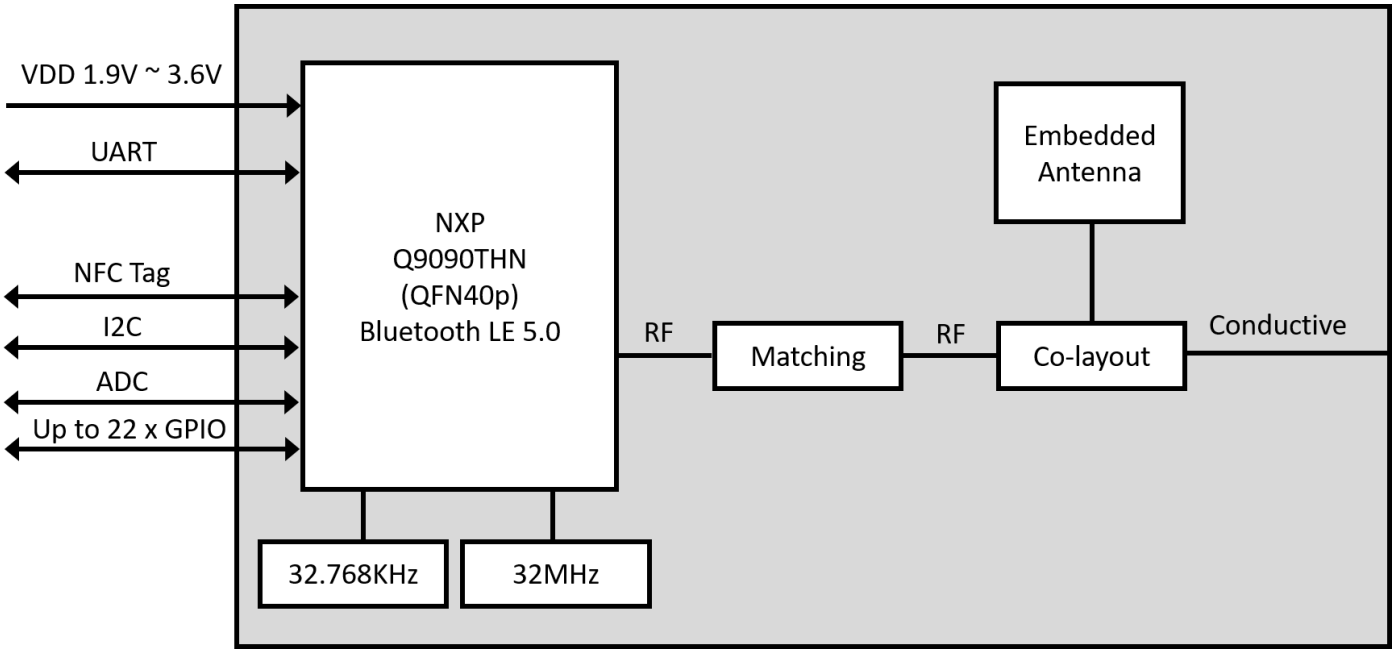
1.2 Block Diagram



AW-CU480 BLOCK DIAGRAM

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1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	Bluetooth Low Energy 5.0 Module (Stamp LGA)
Major Chipset	QN9090THN (QFN 40p)
Host Interface	BT ● UART
Dimension	15mm x 19.615mm x 2.45mm (Tolerance remarked in mechanical drawing)
Form factor	Stamp LGA Module
Antenna	Main：Bluetooth → TX/RX
Weight	1.2g

1.3.2 Bluetooth

Features	Description
Bluetooth Standard	Bluetooth Low Energy 5.0
Bluetooth VID/PID	N/A
Frequency Rage	2402~2480MHz
Modulation	GFSK (1Mbps), Π/4 DQPSK (2Mbps) and 8DPSK (3Mbps)
Output Power (Board Level Limit)*	
Receiver Sensitivity	

	Min	Typ	Max	Unit
Low Energy (1MHz)	8	10	12	dBm
Low Energy (2MHz)	8	10	12	dBm

	Min	Typ	Max	Unit
Low Energy (1MHz)		-94	-91	dBm
Low Energy (2MHz)		-90	-87	dBm

* If you have any certification questions about output power please contact FAE directly.

1.3.3 Operating Conditions

Features	Description
Operating Conditions	
Voltage	Power supply for host: 1.9V ~ 3.6V

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Operating Temperature	-40℃~ 85℃
Operating Humidity	less than 85%R.H.
Storage Temperature	-40℃~ 125℃
Storage Humidity	less than 60%R.H.
ESD Protection	
Human Body Model	3KV
Changed Device Model	500V

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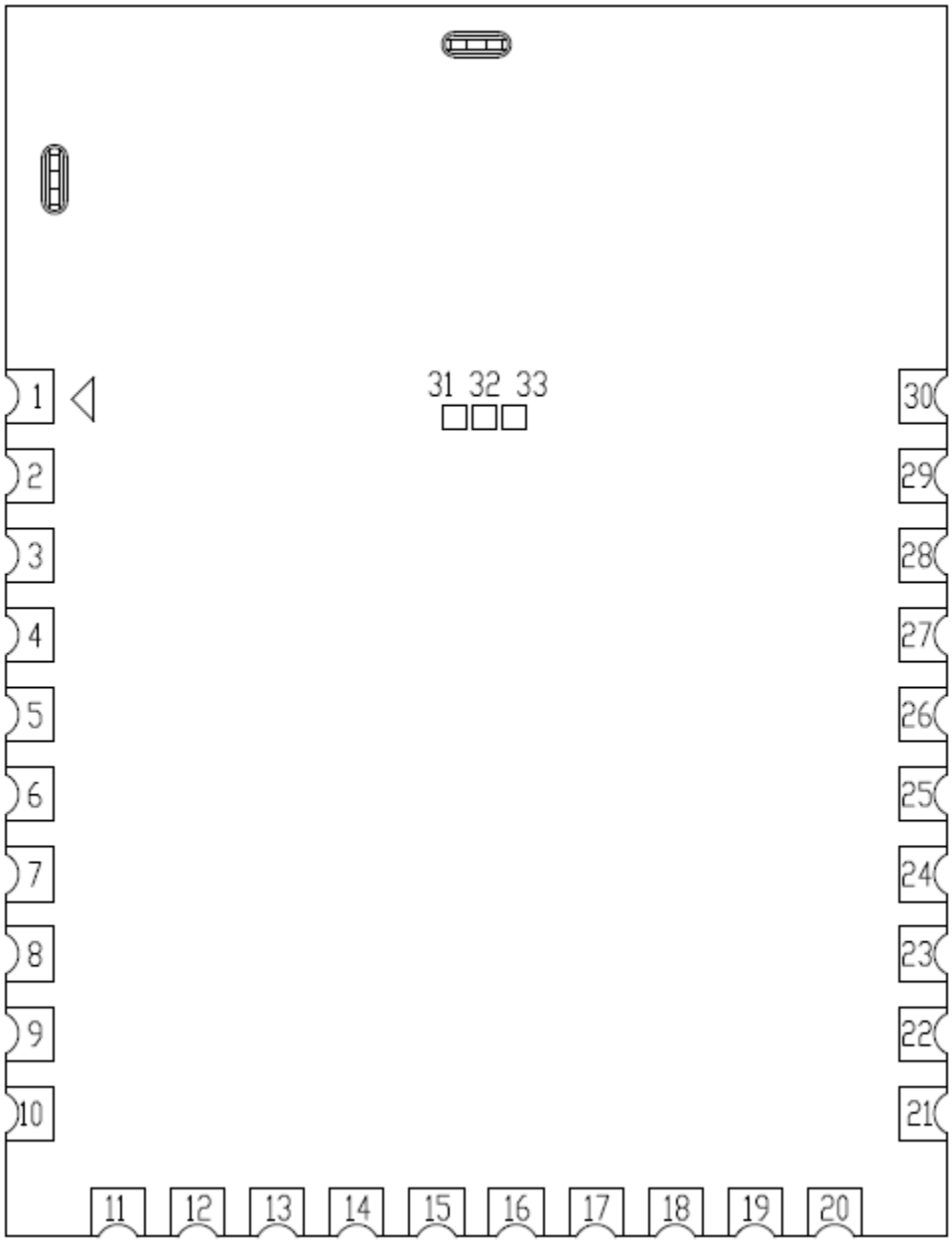
2. Pin Definition

2.1 Pin Map



AW-CU480 Pin Map (Top View)

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2.2 Pin Table

Pin No	Definition	Basic Description	Voltage	Type
1	LB	NFC tag antenna input B		
2	LA	NFC tag antenna input A		
3	PIO_0/SPI1_SCK	General Purpose digital Input/ Output 0		IO
4	PIO_1/SPI1_MISO	General Purpose digital Input/ Output 1		IO
5	PIO_2/SPI1_MOSI	General Purpose digital Input/ Output 2		IO
6	PIO_3/SPI1_SSELN0	General Purpose digital Input/ Output 3		IO
7	PIO_4/PWM4-PU	General Purpose digital Input/ Output 4		IO
8	PIO_5/ISP_ENTRY	General Purpose digital Input/ Output 5		IO
9	PIO_6/PWM6-PD	General Purpose digital Input/ Output 6		IO
10	PIO_7/PWM7-PD	General Purpose digital Input/ Output 7		IO
11	PIO_8/USART0_TXD	UART0_TX		IO
12	PIO_9/USART0_RXD	UART0_RX		IO
13	PIO_10/I2C0_SCL	General Purpose digital Input/ Output 10		IO
14	PIO_11/I2C0_SDA	General Purpose digital Input/ Output 11		IO
15	PIO_12/SWCLK	General Purpose digital Input/ Output 12		IO
16	PIO_13/SWDIO	General Purpose digital Input/ Output 13		IO
17	PIO_14/ADC0	General Purpose digital Input/ Output 14		IO
18	PIO_15/ADC1	General Purpose digital Input/ Output 15		IO
19	PIO_16/SPIFI_CSN	General Purpose digital Input/ Output 16		IO
20	GND	Ground.		GND
21	GND	Ground.		GND

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22	VDD	Power supply	1.9 ~3.6V	VDD
23	PIO_17/SPIFI_IO3	General Purpose digital Input/ Output 17		IO
24	PIO_18/SPIFI_CLK	General Purpose digital Input/ Output 18		IO
25	PIO_19/SPIFI_IO0	General Purpose digital Input/ Output 19		IO
26	PIO_20/SPIFI_IO2	General Purpose digital Input/ Output 20		IO
27	PIO_21/SPIFI_IO1	General Purpose digital Input/ Output 21		IO
28	RSTN	Reset. Active low.		I
29	GND	Ground.		GND
30	GND	Ground.		GND
31	GND	Ground.		GND
32	RF	RF out.		O
33	GND	Ground.		GND

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3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Typical	Max	Unit
V_{LX}	LA and LB pin voltage	-0.3		4.6	V_{peak}
V_{DD}	Supply voltage DCDC input	-0.3		3.96	V
V_{IO}	IO pins voltage	-0.3		3.96	V
V_{RST}	RSTIN voltage	-0.3		3.96	V
V_{ADC}	ADC pins voltage	-0.3		3.96	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
VDD	DCDC voltage	1.9	--	3.6	V

3.3 IO Pin Characteristics

Symbol	Parameter	Min	Typical	Max	Unit
$R_{pu(int)(PIO)}$	Internal pull-up resistance on pins PIOx[1]	40	50	60	kΩ
$R_{pu(int)(RSTIN)}$	Internal pull-up resistance on pins RSTIN	40	50	60	kΩ
$R_{pdn(int)(PIO)}$	Internal pull-down resistance on pins PIOx[1]	40	50	60	kΩ

[1] All PIO except RSTIN (reset), PIO10 and PIO11 (I2C function).

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3.4 SPI timing

3.4.1 SPI master timing

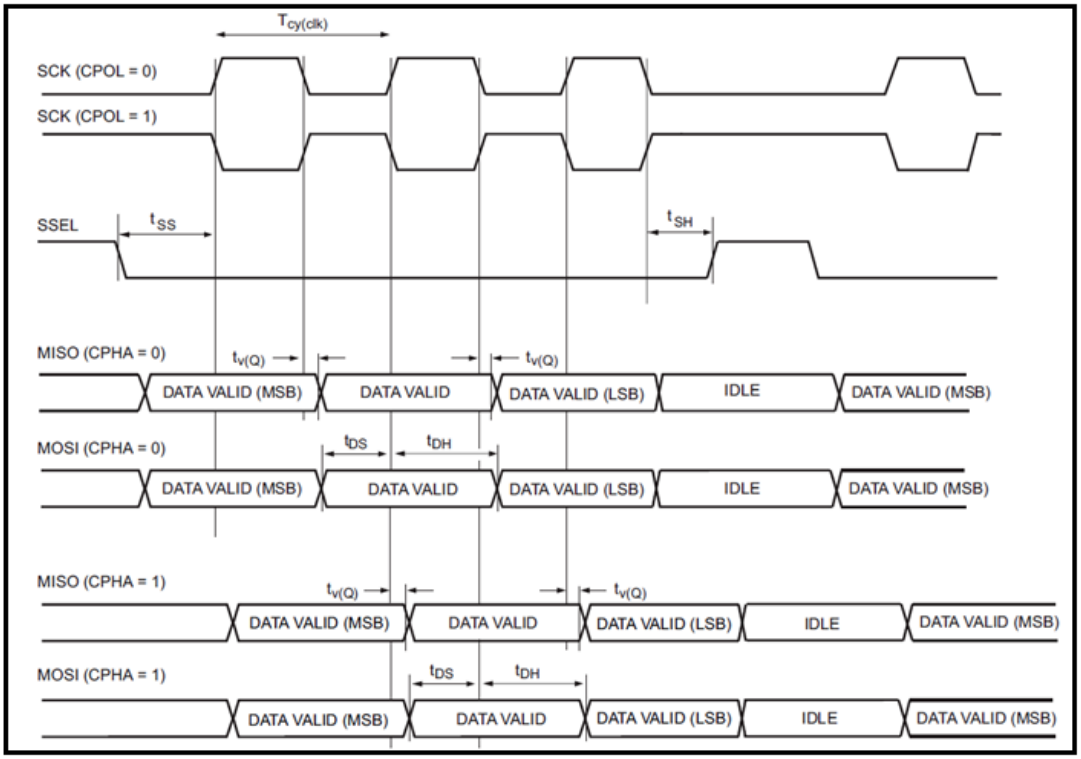
Symbol	Parameter	Min	Typical	Max	Unit
	Duty cycle	45	50	55	%
t_{SS}	SSEL low before SCK edge[1]	1	--	--	SCK cycles
t_{SH}	SSEL low after last SCK edge[2]	0.5	--	--	SCK cycles

3.4.2 SPI slave timing

Symbol	Parameter	Min	Typical	Max	Unit
t_{DS}	Data set-up time	12	--	--	ns
t_{DH}	Data hold time	5	--	--	ns
$t_{V(Q)}$	Data output valid time	0	--	35	ns
$t_{cy(SCK)}$	SCK frequency	--	--	8	MHz
t_{SS}	SSEL low before SCK edge[1]	1	--	--	ns
t_{SH}	SSEL low after last SCK edge[2]	0.5	--	--	ns

[1] Pre-delay can be configured to increase this time in steps of 1 SCK cycle

[2] Post-delay can be configured to increase this time in steps of 1 SCK cycle



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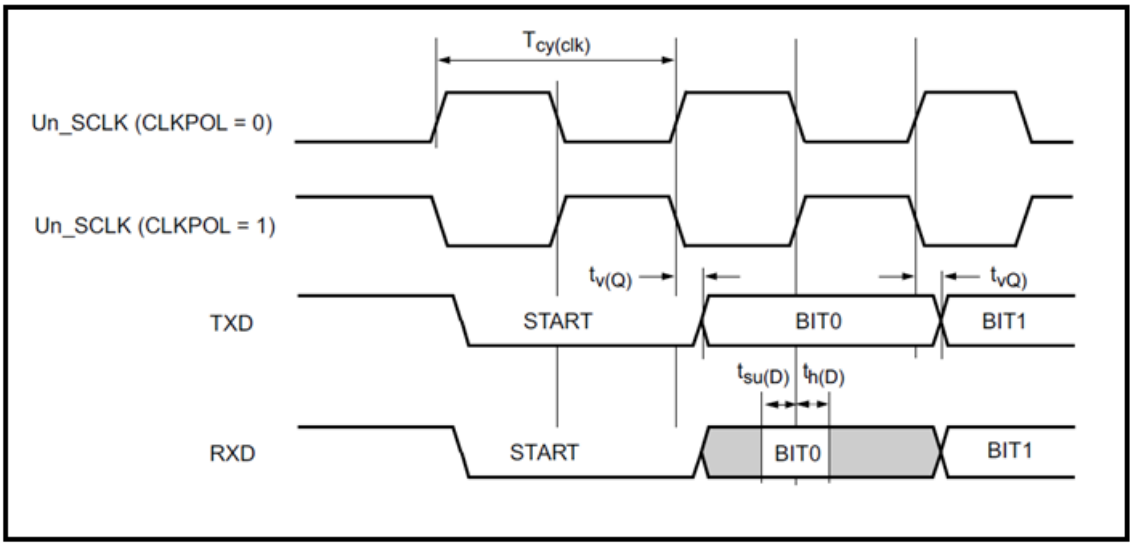
3.5 USART timing

3.5.1 USART master timing

Symbol	Parameter	Min	Typical	Max	Unit
$t_{SU(D)}$	Data set-up time	45	--	--	ns
$t_{h(D)}$	Data hold time	5	--	--	ns
$t_{V(Q)}$	Data output valid time	0	--	25	ns
$t_{cy(SCK)}$	SCK frequency	--	--	5	MHz

3.5.2 USART slave timing

Symbol	Parameter	Min	Typical	Max	Unit
$t_{SU(D)}$	Data set-up time	5	--	--	ns
$t_{h(D)}$	Data hold time	5	--	--	ns
$t_{V(Q)}$	Data output valid time	0	--	55	ns
$t_{cy(SCK)}$	SCK frequency	--	--	5	MHz



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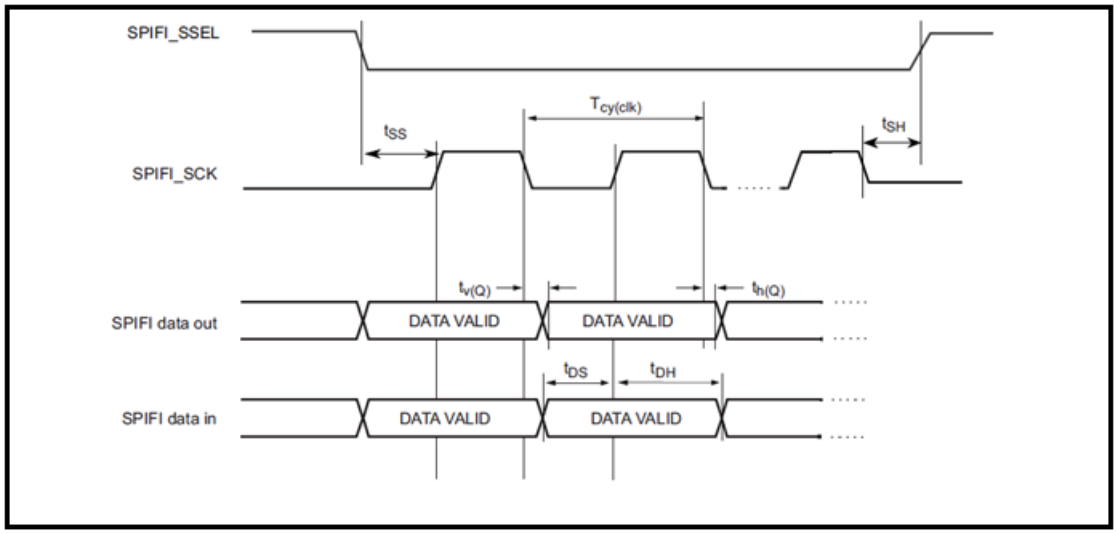
3.6 SPIFI timing

3.6.1 SPIFI timing

Symbol	Parameter	Min	Typical	Max	Unit
$t_{cy(SCK)}$	SCK frequency	30	--	--	ns
t_{DS}	Data set-up time	3	--	--	ns
t_{DH}	Data hold time	3	--	--	ns
$t_{V(Q)}$	Data output valid time	--	--	5	ns
$t_{H(Q)}$	Data output hold time	-10.5	--	--	ns
	Duty cycle	40	--	60	%
t_{SS}	SSEL low before SCK edge[1]	0.5	--	--	SCK cycles
t_{SH}	SSEL low after last SCK edge[2]	0.5	--	--	SCK cycles



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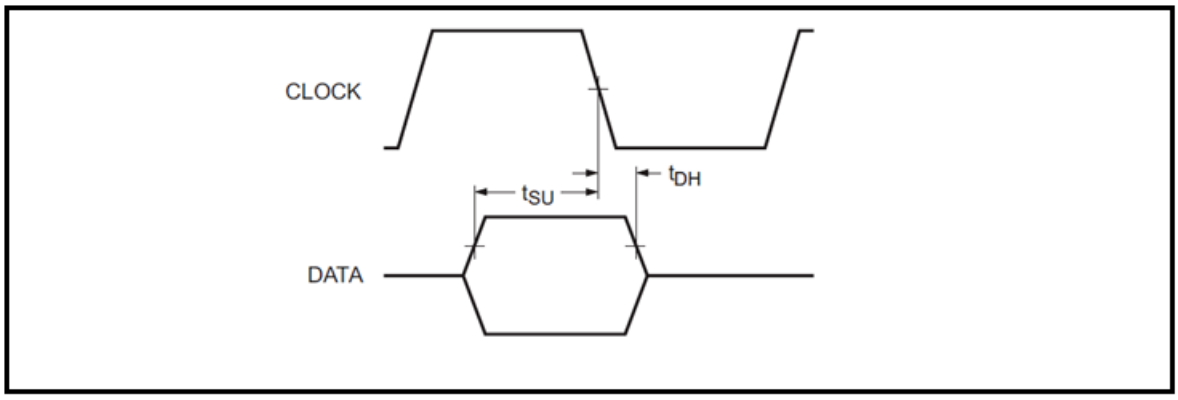
3.7 PWM timing

Symbol	Parameter	Min	Typical	Max	Unit
t_{SK}	Output skew time	0	--	10	ns

3.8 DMIC timing

Symbol	Parameter	Min	Typical	Max	Unit
$t_{cy(SCK)}$	DMIC CLK frequency	--	--	2	MHz
	Duty cycle	48	--	52	%
t_{DS}	Data set-up time	25	--	--	ns
t_{DH}	Data hold time	1	--	--	ns



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3.9 Power Consumption*

3.9.1 Bluetooth

No.	Item	VDD_IN=3.0V(PIN_22)		
		Max.	Avg.	Unit.
1	Deep power-down (everything is powered off, wake-up on HW reset only)	0.539	0.245	uA
2	Power-Down (wake-up on HW reset or an IO event, wake-up timer ON, 32 kHz FRO on, no SRAM retention).	1.27	0.863	uA
3	Deep Power-Down-IO. Everything is powered off, wake-up on HW reset only or an event on any of the 22 GPIOs and NTAG interrupt) (for K32W061)	0.656	0.359	uA
4	Sleep	2.62	2.23	mA
5	RX Idle	2.67	2.37	mA
6	Advertising mode	2.28	1.95	uA

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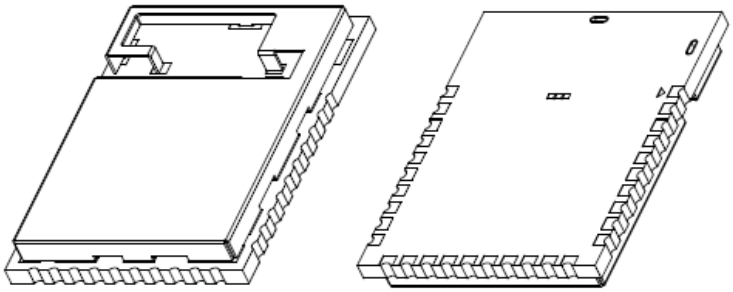
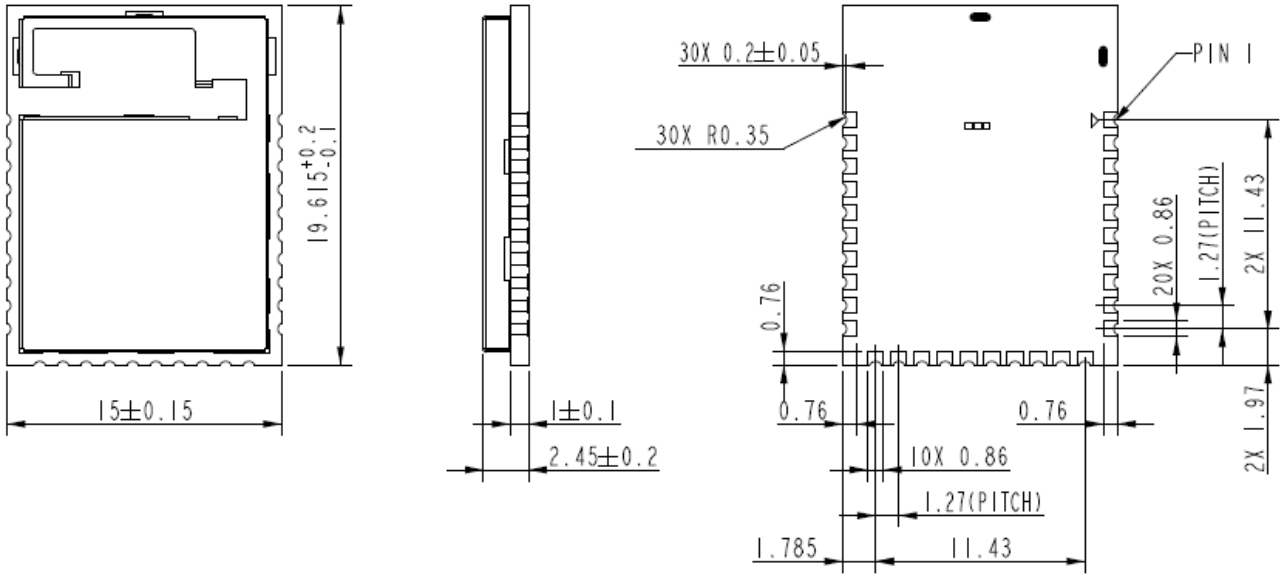
4. Mechanical Information

4.1 Mechanical Drawing





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5. Packaging Information

Tape reel = 1 Box = 700 pcs

Carton = 3 Boxes = 2,100 pcs

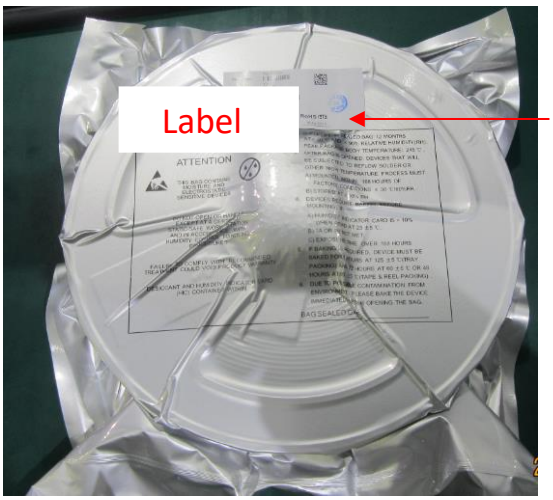
5.1 Tape & Reel Picture

DESICCANT

HUMIDITY INDICATOR CARD

AFFIX PACKING LABEL

5.2 Packing Picture



AFFIX PACKING LABEL

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5.3 Inside of Inner Box Picture

PINK BUBBLE WRAP

5.4 Inner Box Picture

AFFIX PACKING LABEL

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5.5 Inside of Carton Picture

1 Carton = 3 Boxes

5.6 Carton and Label Picture

AFFIX SHIPPING LABEL

AFFIX PACKING LABEL

AFFIX BOX LABEL

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